REMARKS

Claims 1-26 are pending. The Applicants respectfully request reconsideration and allowance of this application in view of the above amendments and the following remarks.

Claims 16, 17, 23 and 24 are objected to because of informalities. The phrase "no current" has been changed to "a maximum of 0.1A." Support for this amendment may be found in the specification at, for example, page 19, lines 14-21. Therefore, the Applicants respectfully request the withdrawal of the objections to claims 16, 17, 23 and 24.

Claims 1-26 stand rejected under 35 U.S.C. 103(a) over Eto et al. (U.S. 6,201,378) in view of the admitted prior art. This rejection is respectfully traversed.

Eto discloses in FIG. 1 a semiconductor integrated circuit that includes a detecting circuit for detecting the difference between the reference voltage V_{ref} and the output voltage V_{pr}. When the output voltage V_{pr} becomes lower than the reference voltage V_{ref}, the first operational amplifier 1 outputs an amplified voltage of "L" level. When the output voltage V_{pr} becomes higher than the reference voltage V_{ref}, the first operational amplifier 1 outputs an amplified voltage of "H" level. The amplified voltage of "L" level or "H" level is applied to the gate of the PMOS transistor 3, as is shown in FIG. 7.

When the amplified voltage of "L" level is applied, that is, when the output voltage of V_{pr} is lower than the reference voltage V_{ref}, the first output transistor 3 (PMOS transistor 3) is turned on. This causes the output voltage V_{pr} to rise until the output voltage becomes equal to the level of the reference voltage V_{ref}. At this time, the second output transistor 4 (NMOS transistor 4) is turned off because of the amplified voltage of "L" level. When the amplified voltage "H" level is applied to PMOS transistor 3, that is, when the output voltage V_{pr} is higher than the reference voltage V_{ref}, the second output transistor 4 realized by an NMOS transistor 4 is turned on. This

causes the output voltage V_{pr} to be lowered until the output voltage becomes equals to the level of the reference voltage V_{ref}. At this time, the PMOS transistor 3 is turned off because of the amplified voltage of "H" level (col. 12, lines 30-57). However, Eto neither teaches nor suggests a power consumption reduction aspect of the detecting circuit. To the contrary, Eto teaches the constant operation of the PMOS transistor to increase V_{pr} to V_{ref} and constant NMOS operation to lower V_{pr} to V_{ref}. To increase V_{ref}, the PMOS transistor is turned on to increase V_{pr} to the appropriate level. Once $V_{pr}=V_{ref}$ is reached, the NMOS transistor is turned off but the PMOS transistor is not, to maintain $V_{pr}=V_{ref}$. Similarly, to lower the V_{ref}, the NMOS transistor is turned on to lower V_{pr} to the appropriate level. Once $V_{pr}=V_{ref}$ is reached, the PMOS transistor is turned off but the NMOS transistor is not, to maintain $V_{pr}=V_{ref}$.

The admitted prior art (APA), i.e., FIG. 10 in the present application, discloses a switching element 4 but neither teaches nor suggests a power consumption reduction circuit, as shown in FIG. 10 (Prior Art). For example, FIG. 10 does not show a voltage detector between transistors T1 and T2 that can detect the transistors' operational state and adjust power consumption accordingly.

The present invention as recited in claim 1 overcomes the deficiencies of the combination of Eto in view of APA by reciting a drive circuit for driving a switching element comprising a voltage detector and a low side switching circuit that is controlled to be turned off when the voltage detected by the voltage detector is lower than that of the off decision voltage. By turning off both transistors T11 and T21 at all times other than switching between "H" and "L" levels, i.e., when the circuit is in steady state operation, the drive circuit of the present invention decreases power consumption by amounts consumed by the transistors T11 and T21 (page 27, lines 8-13 and FIG. 2). Therefore, as the combination of Eto et al. in view of APA fails to

render claim 1 obvious, the Applicants respectfully request the withdrawal of the 35 U.S.C. 103(a) rejection of claim 1.

Claims 2-5, 16, 18 and 20 are dependent from, either directly or indirectly, claim 1 which is believed to be in allowable form. Therefore, claims 2-5, 16, 18 and 20 are believed to be in allowable form. The Applicants respectfully request the 35 U.S.C. 103(a) rejection of claims 2-5, 16, 18 and 20 be withdrawn.

Regarding claim 6, the 35 U.S.C. 103(a) rejection is respectfully traversed. As already discussed, Eto describes a semiconductor integrated circuit that includes a detecting circuit for detecting the difference between the reference voltage V_{ref} and the output voltage V_{pr}. However, Eto neither teaches nor suggests a power consumption reduction aspect of the detecting circuit.

The APA discloses a switching element 4 but neither teaches nor suggests a power consumption reduction circuit.

The present invention overcomes the deficiencies of the combination of the Eto in view of APA by reciting a drive circuit for driving a switching element comprising a voltage detector and a high side switching circuit which is controlled to be turned off when the voltage detected by the voltage detector is higher than that of the on decision voltage. By turning off both transistors T11 and T21 at all times other than switching between "H" and "L" levels, i.e., when the circuit is in steady state operation, the present invention decreases power consumption by amounts consumed by the transistors T11 and T21 (page 27, lines 8-13 and FIG. 2). Therefore, as the combination of Eto et al. in view of APA fails to render claim 6 obvious, the Applicants respectfully request the withdrawal of the 35 U.S.C. 103(a) rejection of claim 6.

Claims 7-10, 21, 23 and 25 are dependent from, either directly or indirectly, on claim 6, which is believed to be in allowable form. Therefore, claims 7-10, 21, 23 and 25 are believed to be in allowable form. The Applicants respectfully request the 35 U.S.C. 103(a) rejection of claims 7-10, 21, 23 and 25 be withdrawn.

Regarding claim 11, the 35 U.S.C. 103(a) rejection of claim 11 is respectfully traversed. As already discussed, Eto describes a semiconductor integrated circuit that includes a detecting circuit for detecting the difference between the reference voltage V_{ref} and the output voltage V_{pr}. However, Eto neither teaches nor suggests a power consumption reduction aspect of the detecting circuit.

The APA discloses a switching element 4 but neither teaches nor suggests a power consumption reduction circuit.

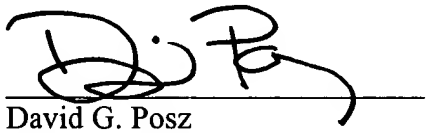
The present invention overcomes the deficiencies of the combination of the Eto in view of APA by reciting a drive circuit for driving a switching element comprising a voltage detector which includes a low side switching circuit which is controlled to be turned off when the voltage detected by the voltage detector is lower than that of the off decision voltage and a high side switching circuit which is controlled to be turned off when the voltage detected by the voltage detector is higher than the on decision voltage. By turning off both transistors T11 and T21 at all times other than switching between "H" and "L" levels, i.e., when the circuit is in steady state operation, the present invention decreases power consumption by amounts consumed by the transistors T11 and T21 (page 27, lines 8-13 and FIG. 2). Therefore, as the combination of Eto et al. in view of APA fails to render claim 11 obvious, the Applicants respectfully request the withdrawal of the 35 U.S.C. 103(a) rejection of claim 11.

Claims 12-15, 17, 19, 22, 24 and 26 are dependent from, either directly or indirectly, claim 11, which is believed to be in allowable form. Therefore claims 12-15, 17, 19, 22, 24 and 26 are believed to be in allowable form. The Applicants respectfully request the 35 U.S.C. 103(a) rejection of claims 12-15, 17, 19, 22, 24 and 26 be withdrawn.

In view of the foregoing, the Applicants respectfully submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the Examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



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